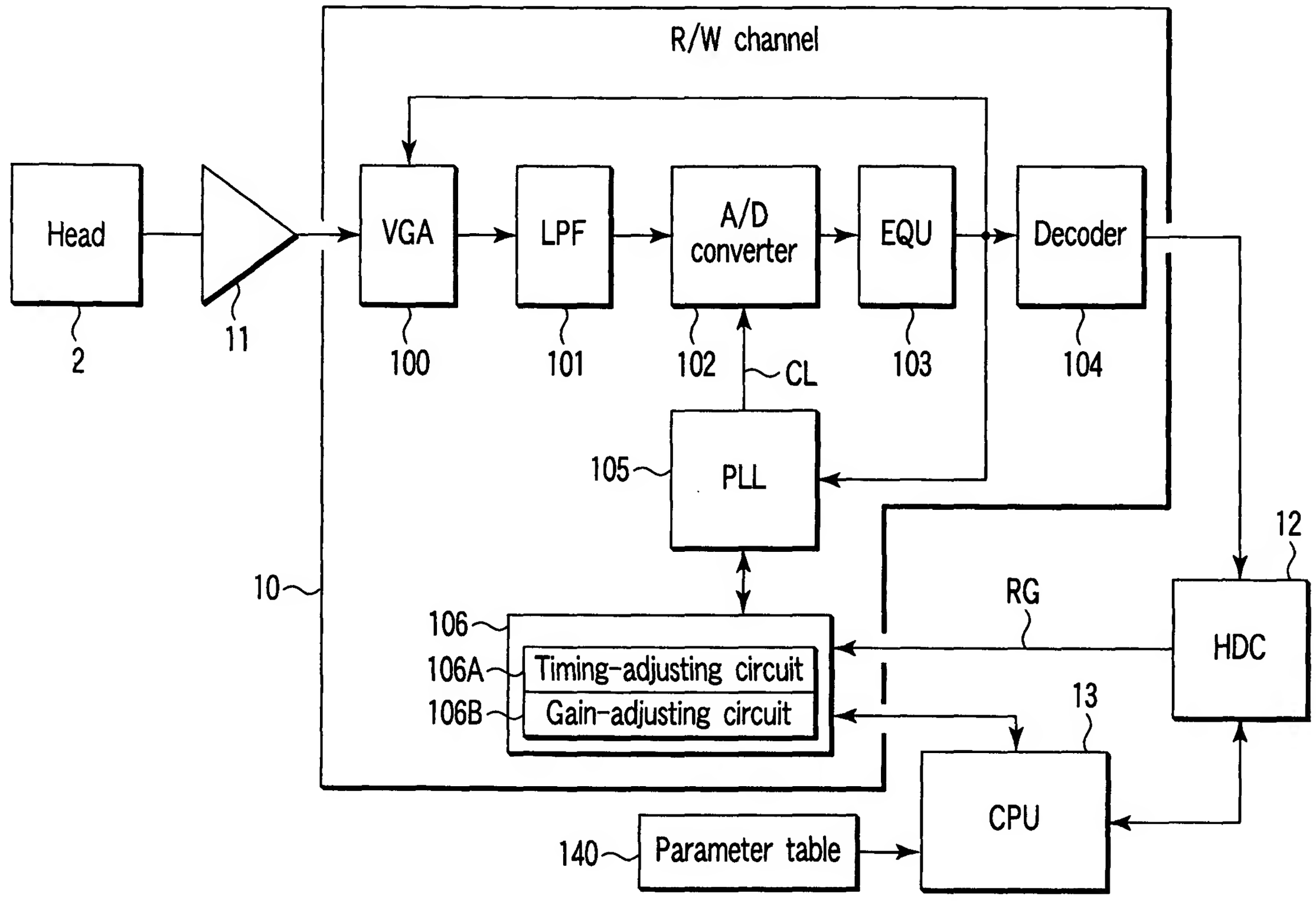
R/W channel
Head
11
2
VGA
100
LPF
101
A/D converter
102
CL
EQU
103
Decoder
104
105
PLL
12
10
RG
HDC
106
106A
Timing-adjusting circuit
106B
Gain-adjusting circuit
13
CPU
140
Parameter table

FIG. 1

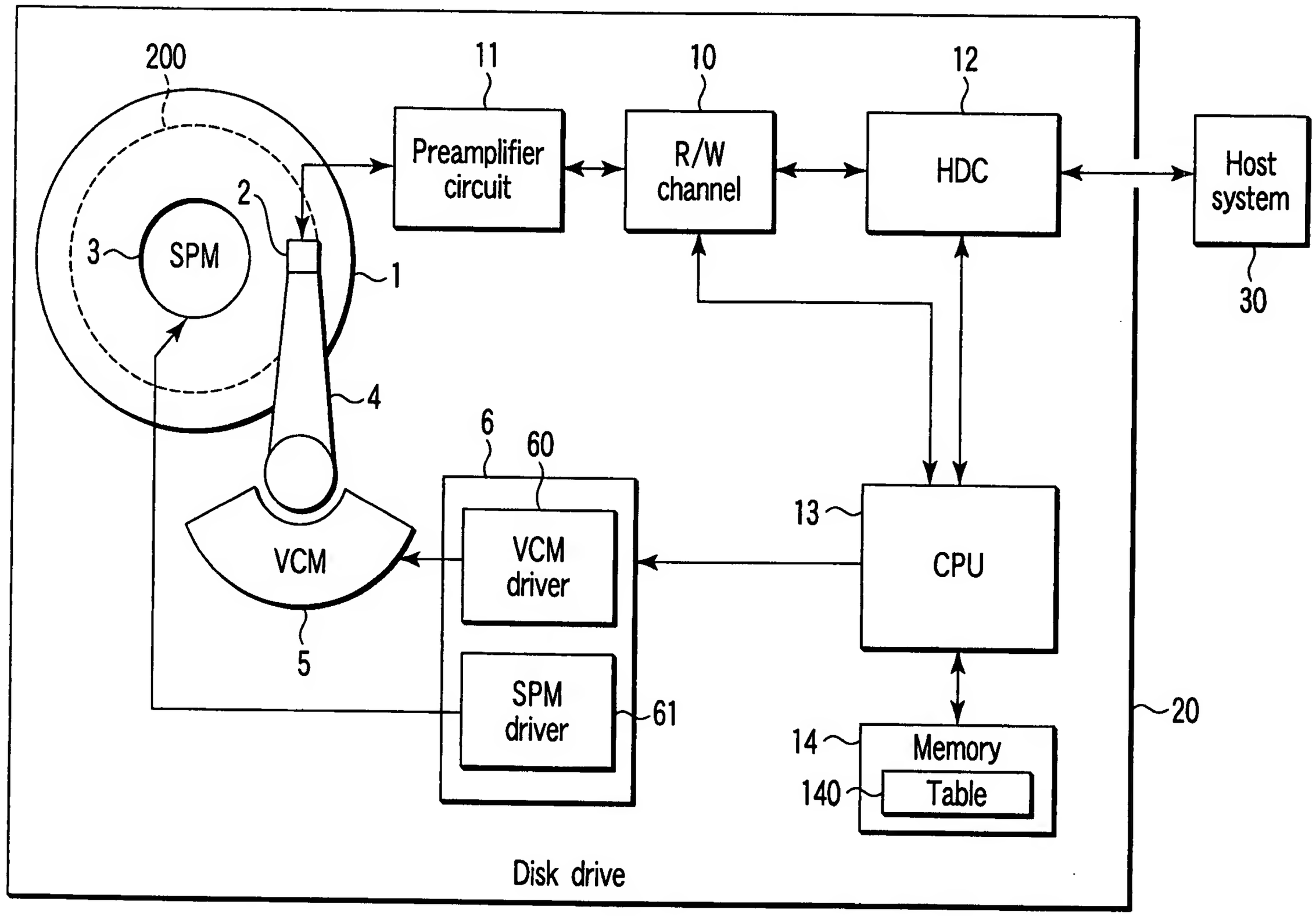
200
11
10
12
Preamplifier circuit
R/W channel
HDC
Host system
30
2
3
SPM
1
4
6
60
VCM
VCM driver
13
CPU
5
SPM driver
61
20
14
Memory
140
Table
Disk drive

FIG. 2

FIG. 3A

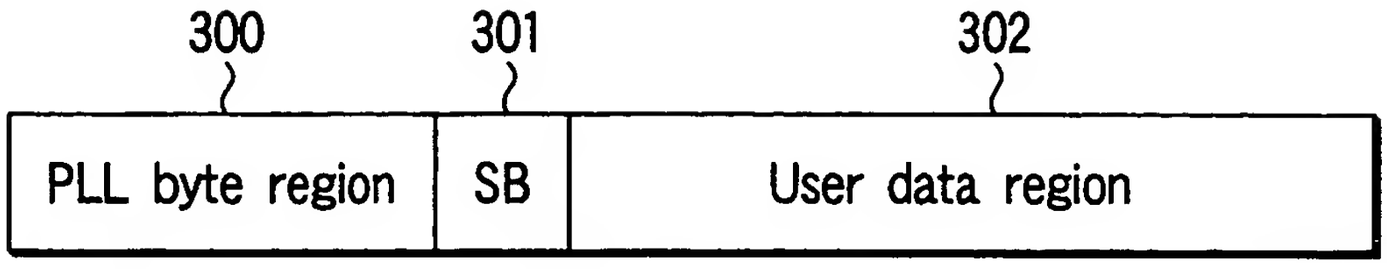

FIG. 3B

FIG. 3C

FIG. 3D

FIG. 4A

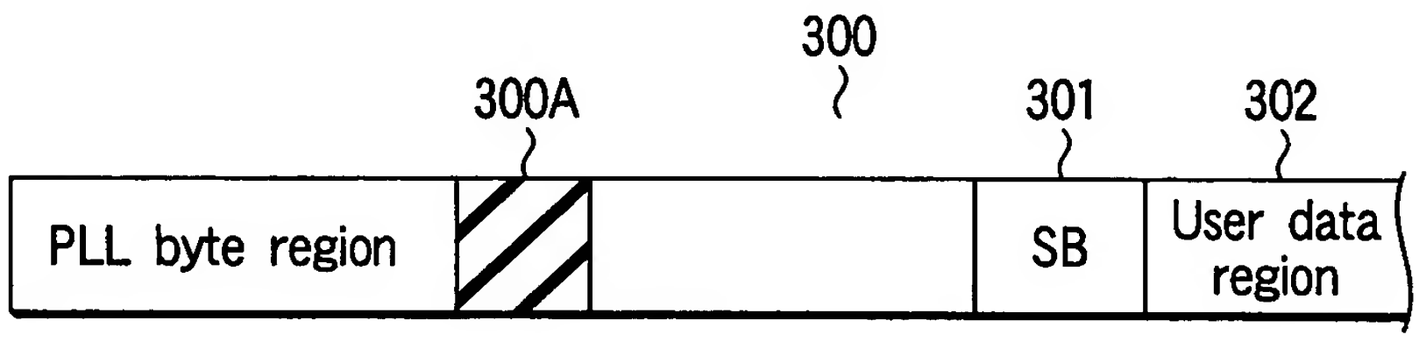

FIG. 4B

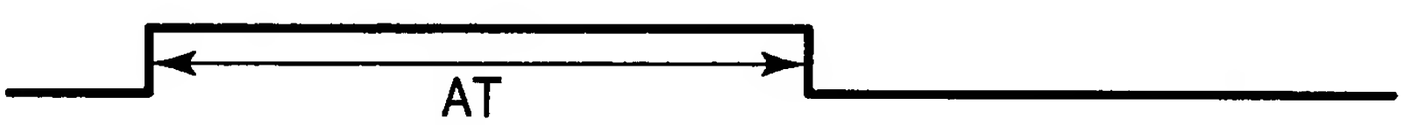

FIG. 4C

FIG. 5A

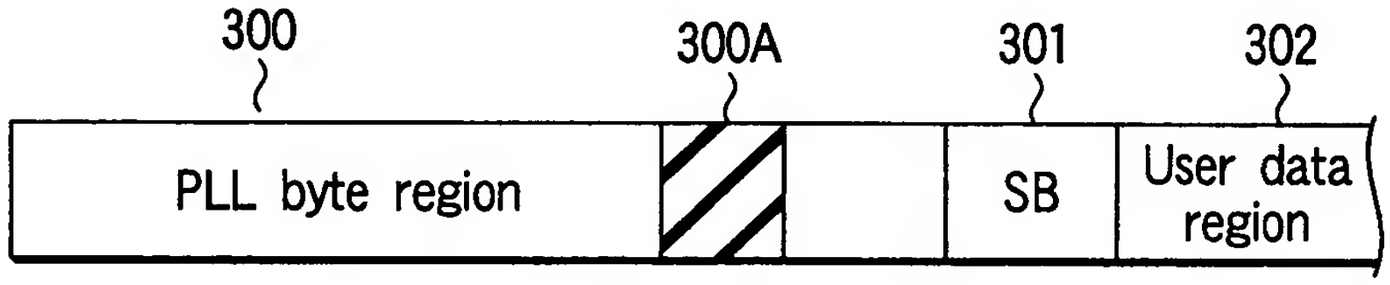

FIG. 5B

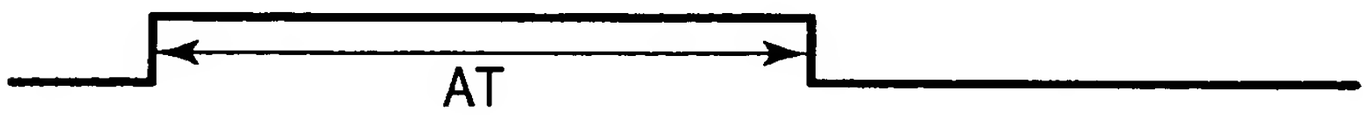

FIG. 5C

FIG. 6A

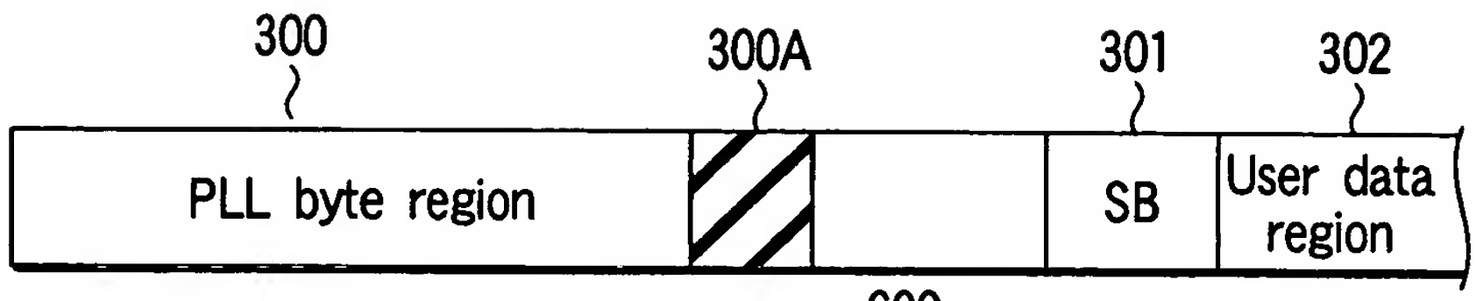

FIG. 6B

FIG. 6C

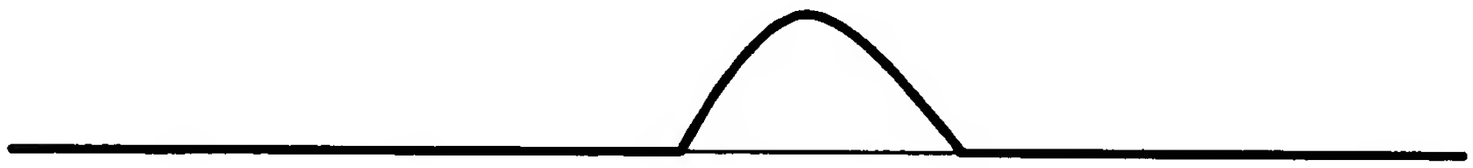

FIG. 7A

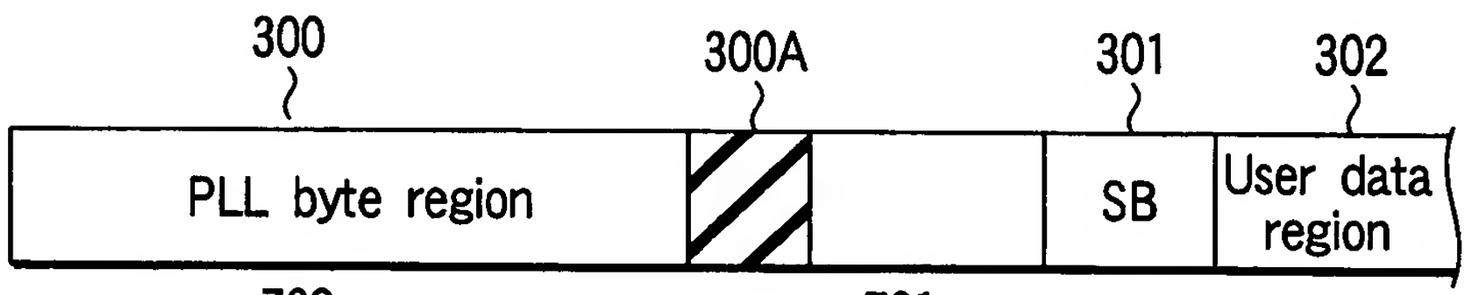

FIG. 7B

FIG. 7C

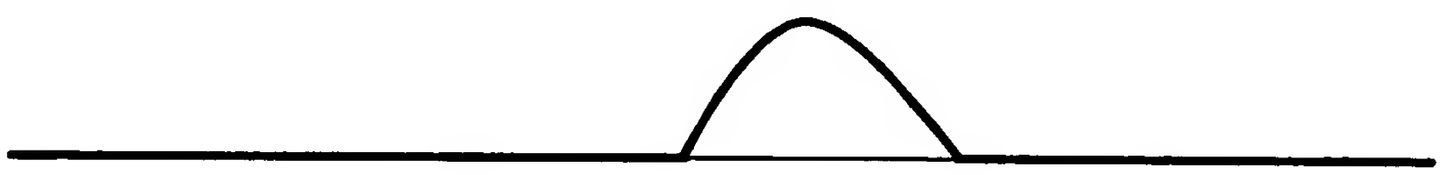

FIG. 8A

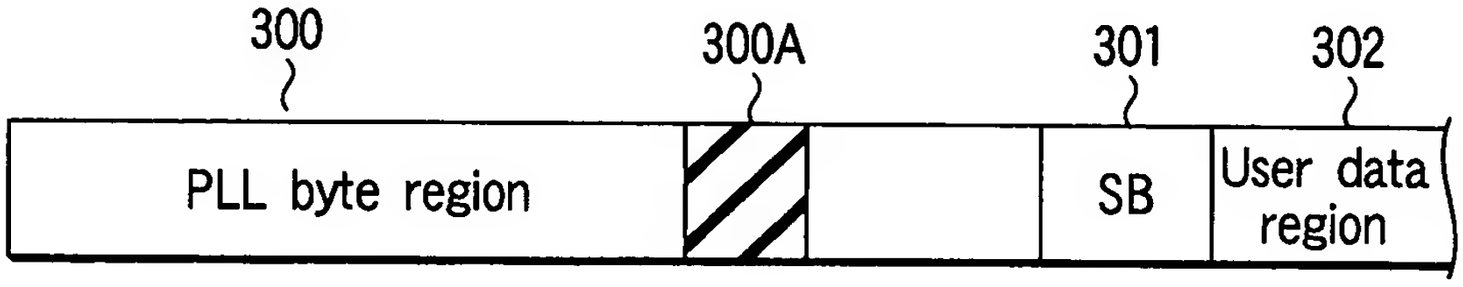

FIG. 8B

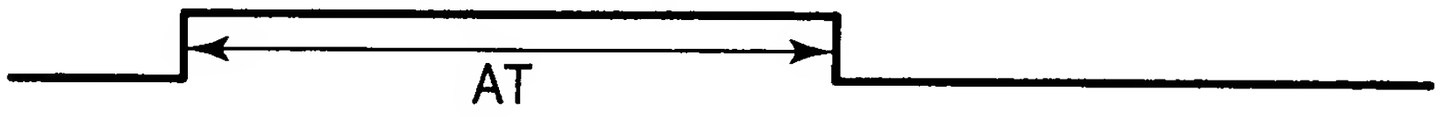

FIG. 8C

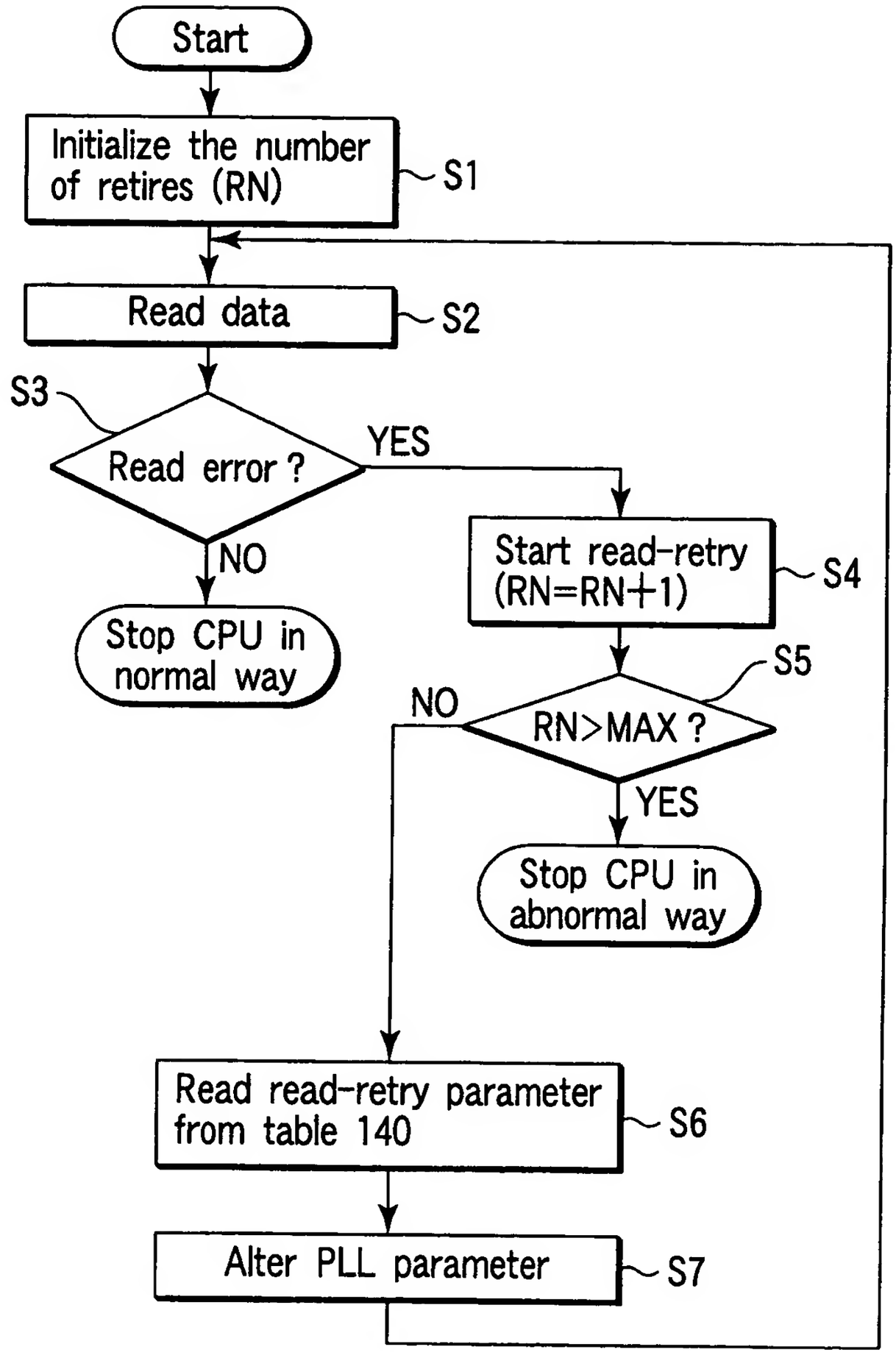
Start
Initialize the number of retires (RN)
S1
Read data
S2
S3
Read error ?
YES
NO
Stop CPU in normal way
Start read-retry (RN=RN+1)
S4
S5
RN>MAX ?
NO
YES
Stop CPU in abnormal way
Read read-retry parameter from table 140
S6
Alter PLL parameter
S7

FIG. 9

Number of retries	Acquisition mode		Gain for tracking mode
	Timing	Gain	
1-128	T1	Ga1	Gt1
129-132	T1	Ga2	Gt1
133-136	T1	Ga3	Gt1
137-140	T2	Ga1	Gt1
141-144	T2	Ga2	Gt1
145-148	T2	Ga3	Gt1
149-152	T3	Ga1	Gt1
153-156	T3	Ga2	Gt1
157-160	T3	Ga3	Gt1
161-192	Identical to those for "129-160"		
193-224	T1	Ga1	Gt2
225-256	T1	Ga1	Gt3

140

FIG. 10

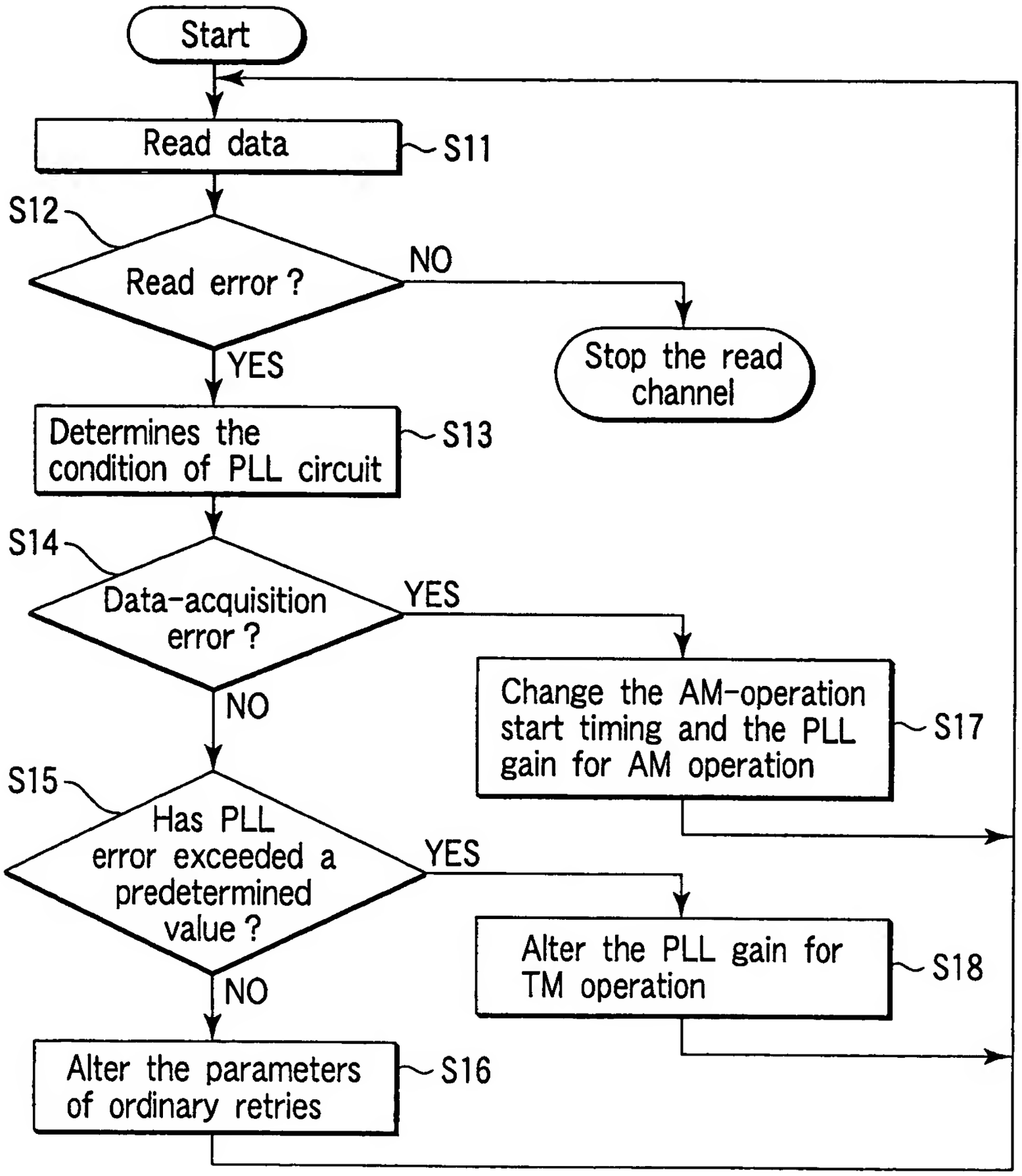
Start
Read data
S11
S12
Read error ?
NO
YES
Stop the read channel
Determines the condition of PLL circuit
S13
S14
Data-acquisition error ?
YES
NO
Change the AM-operation start timing and the PLL gain for AM operation
S17
S15
Has PLL error exceeded a predetermined value ?
YES
NO
Alter the PLL gain for TM operation
S18
Alter the parameters of ordinary retries
S16

FIG. 11

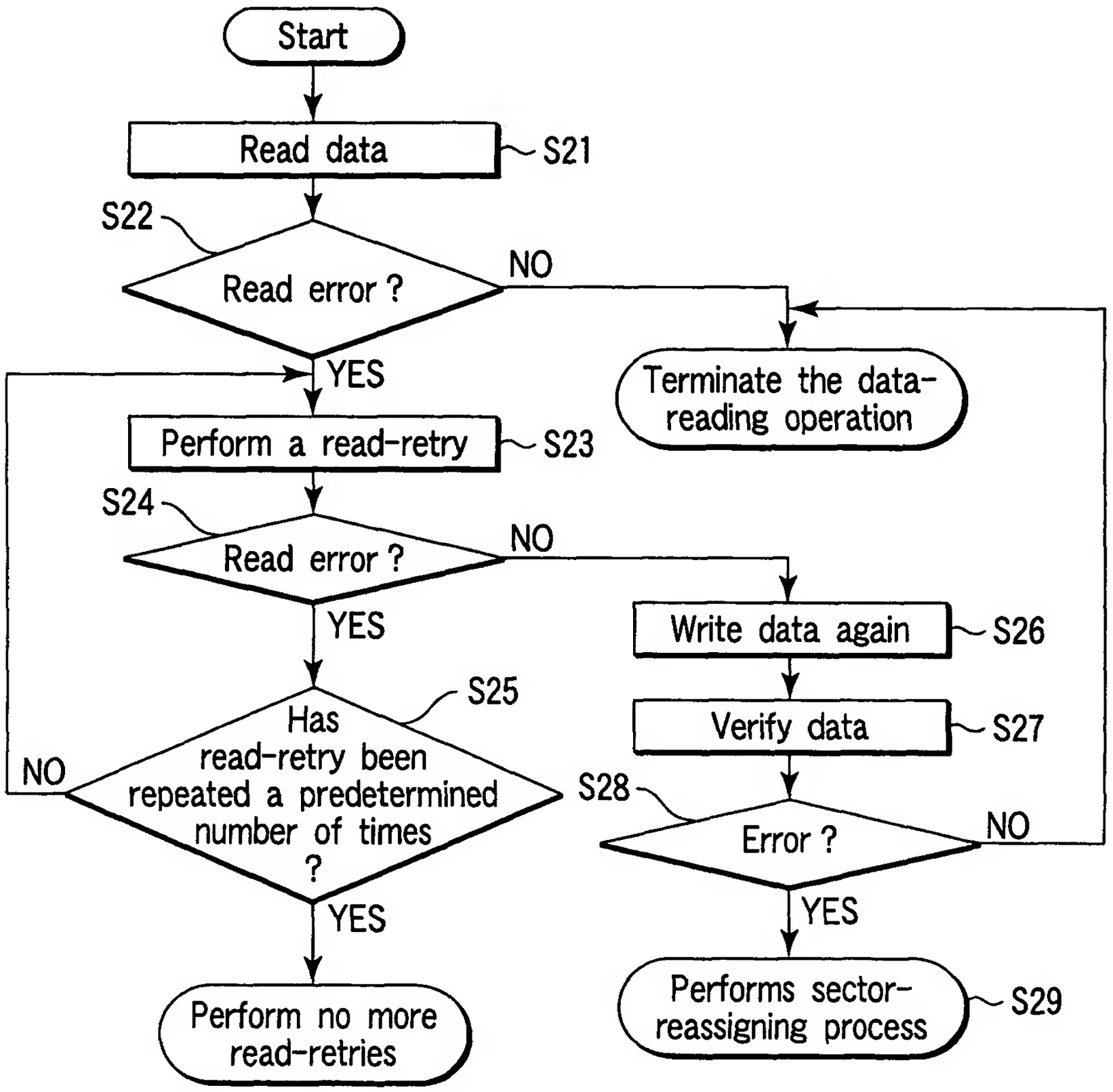
Start
Read data
S21
S22
Read error ?
NO
YES
Terminate the data-reading operation
Perform a read-retry
S23
S24
Read error ?
NO
YES
Write data again
S26
S25
Has read-retry been repeated a predetermined number of times ?
NO
YES
Verify data
S27
S28
Error ?
NO
YES
Perform no more read-retries
Performs sector-reassigning process
S29

FIG. 12